METHOD AND STRUCTURE TO REDUCE CMOS INTER-WELL LEAKAGE

ABSTRACT

A method of forming a semiconductor device with improved leakage control, includes: providing a semiconductor substrate; forming a trench in the substrate; forming a leakage stop implant in the substrate under the bottom of the trench and under and aligned to a sidewall of the trench; filling the trench with an insulator; and forming an N-well (or a P-well) in the substrate adjacent to and in contact with an opposite sidewall of the trench, the N-well (or the N-well) extending under the trench and forming an upper portion of an isolation junction with the leakage stop implant, the upper portion of the isolation junction located entirely under the trench. The leakage control implant is self-aligned to the trench sidewalls.